wherein said output of said detector indicates that said first clock is in advance of said second clock in a phase or said second clock is in advance of said first clock in a phase.

4. (Twice Amended) A semiconductor device comprising a delay locked loop including:

an input buffer receiving an external clock and outputting a first internal clock;

a delay circuit delaying said first internal clock to output a second internal clock;

a detector detecting which of said first and second clocks is advanced in a phase; and

a gray code counter using a gray code, responsive to an output of said detector, for selectively generating a signal to increase an amount of delay of said delay circuit and a signal to decrease said amount of delay of said delay circuit;

wherein said output of said detector indicates that said first clock is in advance of said second clock in a phase or said second clock is in advance of said first clock in a phase.

11. (Twice Amended) A semiconductor device comprising a delay locked loop including:

a first input buffer receiving at least a first external clock and a second external clock complementary in phase to said first external clock, and outputting a first internal clock at the timing of the rising edge of said first external clock when a potential of said first external clock is equal to that of said second external clock;

a second input buffer receiving at least said first and second external clocks, and outputting a second internal clock at the timing of the rising edge of said second external clock when a potential of said first external clock is equal to that of said second external clock;

a first delay circuit delaying said first internal clock to output a third internal clock;

a second delay circuit delaying said second internal clock to output a fourth internal clock;

a detector detecting which of said first and second clocks is advanced in a phase; and

a gray code counter using a gray code, responsive to an output of said detector, for selectively generating a signal to increase an amount of delay of said first delay circuit and an amount of delay of said second delay circuit and a signal to decrease said amount of delay of said delay circuit;

wherein said output of said detector indicates that said first clock is in advance of said second clock in a phase or said second clock is in advance of said first clock in a phase.

14. (Twice Amended) A control method for a system operating in synchronization with a clock, comprising the steps of:

inputting an external clock to an input buffer to generate a first internal clock therefrom;

delaying said first internal clock to output a second internal clock;

detecting which of said first and second clocks is advanced in a phase; and

using a gray code, responsive to a result obtained in the step of detecting, to selectively generate one of a signal to increase an amount of delay to be applied in the step of delaying and a signal to decrease said amount of delay to be applied in the step of delaying;

wherein said result of detecting indicates that said first clock is in advance of said second clock in a phase or said second clock is in advance of said first clock in a phase.